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Ansoft Designer SV project: Using microstrip interdigital capacitors

Very small coupling capacitors are required for bandpass filters in the frequency range between 100MHz and 1GHz, often with values under 0.5pF. Implementing these interdigital capacitors in microstrip gives some advantages. This will be demonstrated in the following practical development.

1.

Introduction

As an introduction into microstrip interdigital capacitors (Fig 1), an extract from the on-line help of the CAD program

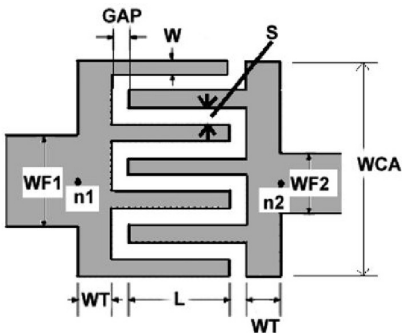


Fig 1: The famous interdigital capacitor. Easily to manufacture but because of the many measurements some work to design.

Properties	Description	Units	Default	Range
N	Number of fingers	none	Required	≥ 2
W	Finger width	m	Required	> 0
S	Finger spacing	m	Required	> 0
L	Length of finger overlap	m	Required	> 0
WT	Terminal strip width	m	Required	≥ 0
WF1	Line width at port 1	m	Required	> 0
WF2	Line width at port 2	m	Required	> 0
WCA	Capacitor width	m	$N*W+(N-1)*S$	$\geq N*W+(N-1)*S$
GAP	Gap between end of finger and terminal strip	m	Required	> 0
sub	Substrate name	none	Required	string
CoSimulator	Simulation engine	none	Circuit	Circuit, Planar EM

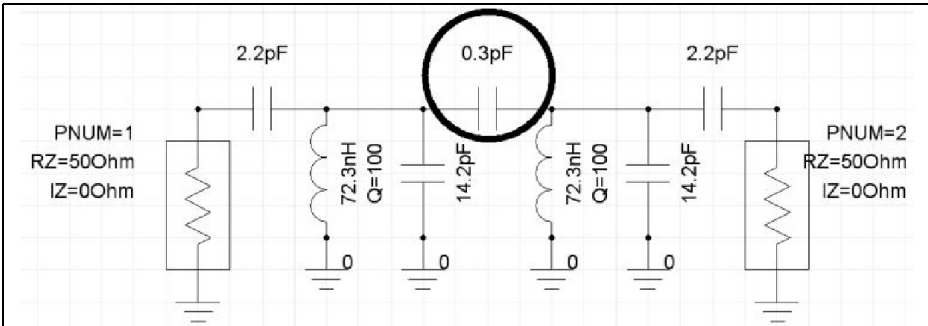


Fig 2: The Ansoft filter tool supplies the finished circuit. The coupling capacitor to be investigated is marked with a circle.

gives all the necessary explanation and details.

The design is not simple, however modern microwave CAD programs facilitate simulation; these should already contain this component in their component library as a microstrip model.

That is the case for the free Ansoft Designer SV software, this is the list of the advantages:

- After optimisation of the PCB layout very small tolerances are achieved leading to good reproducibility of filter parameters without additional components or assembly costs for quantity production.
- No discrete components need to be soldered. These would be difficult to obtain for such small capacitances and exhibit larger tolerances.
- Using high quality printed circuit board material with the smallest losses produces very high quality capacitors that are useful up to more than 10GHz.

is to be designed, built and measured:

- Centre frequency: 145MHz
- Ripple bandwidth: 2MHz
- System resistance Z : 50 Ω
- Filter degree: $n = 2$
- PCB size: 30mm x 50mm
- Tschebyschev narrow bandpass filter type with a Ripple of 0.3dB (coupled resonators)
- PCB material: Rogers RO4003, thickness: 32MIL = 0.813mm, $\epsilon_r = 3.38$, TAND= 0.001
- Housing: Milled aluminium
- Connection: SMA plug

First design:

- Filter coils NEOSID (type 7.1 E with shielding can, $L = 67 - 76$ nH, single coil, quality $Q = 100... 150$, brass adjustment core)
- SMD ceramic capacitors 0805, NP0 material

The filter program contained in Ansoft Designer SV was used. The development of the circuit after the draft and a short optimisation is shown in Fig 2. The further work necessary to produce the finished PCB layout is described in the following article. A prototype was produced and tested using a network analyser to give the measurement results.

The design of the filter using Ansoft Designer SV giving all the steps leading

2.

The project, a 145MHz bandpass filter

A bandpass filter with the following data



to Fig 2 is shown in Appendix 1.

Appendix 2 contains guidance for successful control of the circuit simulation using Ansoft Designer SV.

It will also be helpful to download a copy of the authors tutorial on using Ansoft Designer SV. This is available free of charge in German or English from the web site [1].

To continue with the filter development; a look at the circuit of Fig 2 shows:

- The problematic coupling capacitor $C = 0.3\text{pf}$ is identified by the black circle. The problem is not only the very small capacitance but also the high requirement for accuracy. A deviation of more than 1% gives a noticeable change in the transmission characteristics.
- It was optimised until all remaining capacitors can be realised using standard values, if necessary by parallel connection of several capacitors with different values.

3.

Design procedure for interdigital capacitors with Ansoft Designer SV

3.1. Input problems

The component in the model library is under "Circuit Elements/Microstrip/Capacitor/MSICAPSE". The layout of the interdigital capacitor in series connection is shown in Fig 1. Double click on the circuit symbol to access the list of the dimensions. At the end of the list there is a "MSICAP" button that opens the on-line help with an explanation of the individual inputs and dimensions. Experience is required to make these inputs but if the following rules are used then incorrect inputs will be avoided:

- Set the finger width W to 0.5mm.

This ensures that the design does not become too large and under etching has less effect on the finger width when the PCB is made.

- The gap width S should not be TOO small otherwise the PCB manufacturer complains. A value of 0.25mm can be achieved even in your own workshop. On the other hand it should not be too large because then the capacitance value falls, requiring larger finger lengths or more fingers.
- The number of the fingers and their length specifies the capacitance value. As an example, start with 4 fingers and vary the length of the fingers ensuring that they do not become too large. Set an upper limit of about 8 to 10mm. Instead of making the fingers longer simply increase the number of fingers.

With this data (and the PCB data) a draft design can begin BUT unfortunately the CAD program can make an analysis. That means that all the data and dimensions can be entered and the simulation started but the result will be an S-parameter file of the capacitor. It is only at this point that it is known if the capacitance of the draft capacitor is too large or too small.

Things become more difficult because the circuit diagram of the component has additional capacitors from each end to earth. These two unavoidable parallel capacitors detune the resonant circuits. How can these three capacitances be isolated to optimise the circuit, particularly if the filters are more complex and several interdigital capacitors are used?

3.2. Determination of the pure coupling capacitance

It is a challenge to determine the exact value of the coupling capacitor, but the two parallel capacitors are less difficult to deal with, just make the resonant circuit capacitors smaller in the simulation until the desired transmission curve

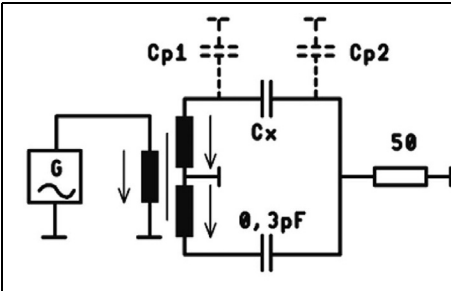


Fig 3: Using an idea from crystal filter technology, this circuit is used to develop the exact value of the interdigital capacitor required.

is achieved. The difference corresponds to the additional parallel capacitance contributed by the interdigital capacitor. Their value is not much different from the actual coupling capacitor.

Sometimes experience helps: e.g. crystal filters in a bridge connection presented a similar problem. In that case the housing capacitance was eliminated using a transformer circuit. The principle applied to the current problem is shown in Fig 3.

The voltage across the two secondary windings are the same magnitude but opposite phases. Thus the voltage, V , across the terminating resistor, R_L , is zero if the two capacitors C_x and C_2 are equal and in this case equal 0.3pF . The

two parallel capacitances C_{p1} and C_{p2} do not play a role when the bridge is balanced thus only the value of C_x is being measured. C_{p1} is parallel to the secondary winding of the transformer and cannot affect the balance of the bridge. Likewise C_{p2} is in parallel with the 50Ω load resistor. In the balanced condition no voltage is developed across the parallel capacitor and the load therefore C_{p2} has no effect on the circuit. This means that the value of interdigital capacitor can be simulated to be exactly the same as the known capacitor C_2 and its parameters will then be known independent of the parallel capacitance values.

The simulation circuit shown in Fig 4 can be developed using Ansoft Designer SV. The transformer can be found in the component library under “Components/Circuit Elements/Lumped/Transformers/TRF1x2” and the series connected interdigital capacitor under “Components/Circuit Elements/Microstrip/Capacitors/MSICAPSE”.

A microwave port with internal resistance of 50Ω feeds a broadband transformer with two secondary windings. The upper coil is connected to the output port by the interdigital capacitor. The opposite phase signal supplied by the lower coil is fed via a second capacitor to the output port.

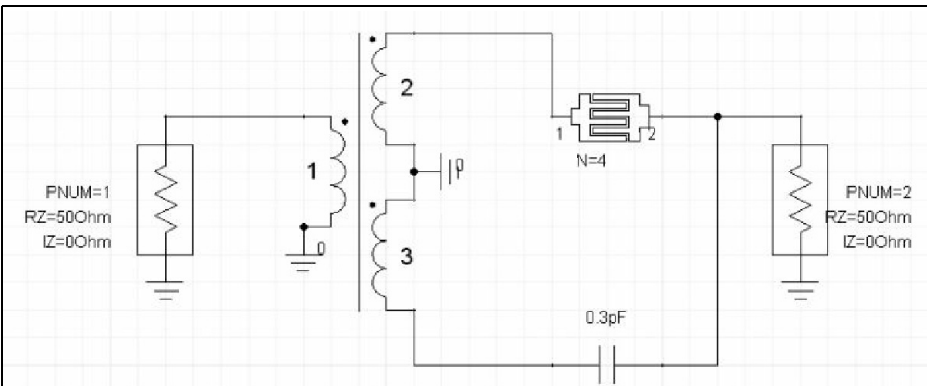


Fig 4: Fig. 3 converted into a form for Ansoft Designer SV simulation.



Fig 5: Somewhat complex: the inputs required for the interdigital capacitor. Take care to examine each value. There is a line that is not visible but should not be forgotten (see text).

Importantly:

This second capacitor must have the same value of 0.3pF (value of the interdigital coupling capacitor required).

The important data for the simulation (and the later draft layout) is entered in the Property Menu of the interdigital capacitor. Double clicking on the symbol in the circuit diagram opens the menu; the entries required are shown in Fig 5.

However there are two important things that are not immediately obvious:

- There is a line missing from the window shown in Fig. 5, this can be found by scrolling down. This line to find is: GAP (between end of finger and terminal strip) = 0.25mm
- The total width “MCA” must be calculated by hand and entered into the relevant field. It should be noted that the units do not automatically default to mm so take care to enter this value otherwise the default will be metres and the simulation will be meaningless.

The above dimension is calculated as

follows: $MCA = 4 \times \text{Finger length} + 3 \times \text{Gap width} = 4 \times 0.5\text{mm} + 3 \times 0.25\text{mm} = 2.75\text{mm}$

Finally the correct PCB material data must be selected. Scroll to the line “SUB” in the open Property Menu for the interdigital capacitor. Click on the button in the second column to open the menu “Select Substrate” and then click on “Edit”. Fill out this form, as shown in Fig 6 for the RO4003 PCB material to be used: thickness = 32MIL = 0.813mm, dielectric constant $\epsilon_r = 3.38$, $\tan \delta = 0.001$, copper coating 35 μm thick and the roughness is 2 μm . Once everything is correct click OK twice to accept the data and close the Property Menu.

Everything is now ready for the simulation. Programme for a sweep from 100MHz to 200MHz with 5MHz increments and look at the results for S21 (If you do not know the individual input steps necessary for Ansoft Designer SV they are described in appendix 2).

The finger lengths of the interdigital capacitor are varied and the simulation run again until the minimum for S21 is found. Now the bridge is balanced and



Substrate Definition

Substrate Name: **R04003**

Substrate Type: **Microstrip**

Dielectric:

H: **0.813** mm

Er: **3.38** TAND: **0.001**

HU: **13** mm

Metalization:

Specify by Material or Resistivity

	Material	Resistivity	Thickness	Unit
1	copper	1.724138	35	um
2				
3				

Roughness: **2** um

OK Cancel

Diagram:

Cover → Metalization → Substrate → Dielectric → Er, TAND → Magnetic → MSAT → MPEM → TANM → Ground

Labels: Air, HU, H, Ground

Fig 6: The data for the Rogers R04003 PCB material are entered correctly into the Property Menu.

the mechanical data for the interdigital capacitor with exactly the correct value can be transferred to the PCB layout. The optimised results are shown Fig 7. The

finger length of 4.25mm gives a minimum for S21 and further refinement is not needed. It is interesting to see the results that the circuit will provide.

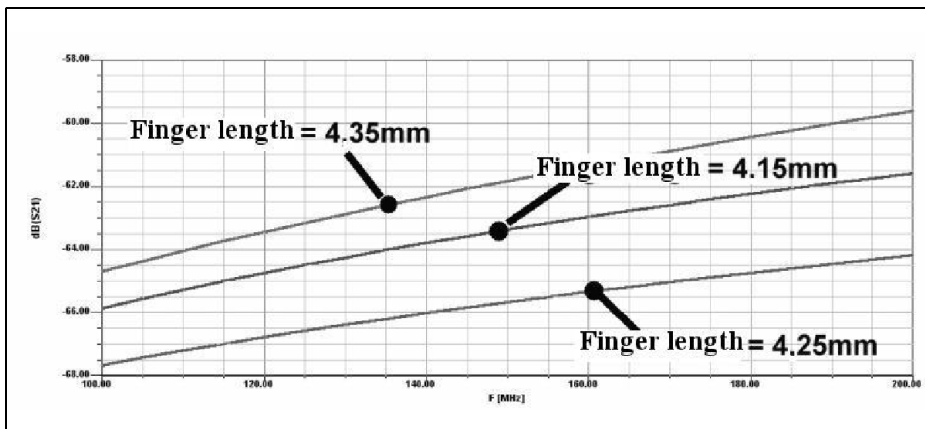


Fig 7: The minimum is easy to recognise: a finger length of 4.25mm gives the correct value for the 0.3pF coupling capacitor.

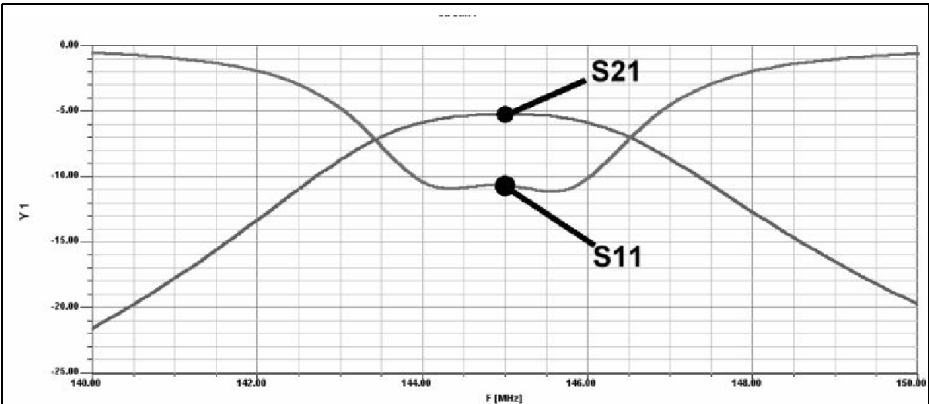


Fig 8: This curve is the goal for this project.

3.3. Completing the circuit

A new project is started with the circuit as shown in Fig 2 from the introduction (with discrete components) and the sweep adjusted from 140 to 150MHz in steps of 100kHz with S11 and S21 displayed. This result is shown in Fig 8. This is the starting point for the following actions, if these result in the same result the you can be quite content.

Replacing the 0.3pF coupling capacitor with the interdigital component that has been designed, this gives the simulation circuit shown in Fig 9. Naturally the results shown in Fig 10 are worse be-

cause the additional parallel capacitances of the interdigital capacitor have not been considered. The parallel capacitors in both resonant circuits must be reduced until the curves of Fig 8 are achieved. Fig 10 shows an additional surprise that apart from the expected shift of the centre frequency from 145MHz to 143.3MHz (caused by the parallel capacitance of the interdigital capacitor) the S11 curve has a diagonal dip. Trying to compensate this effect with different values of two parallel inductances is surprising because as S11 improves, S22 gets worse. This means that this interdigital solution has its peculiarities based on the frequency

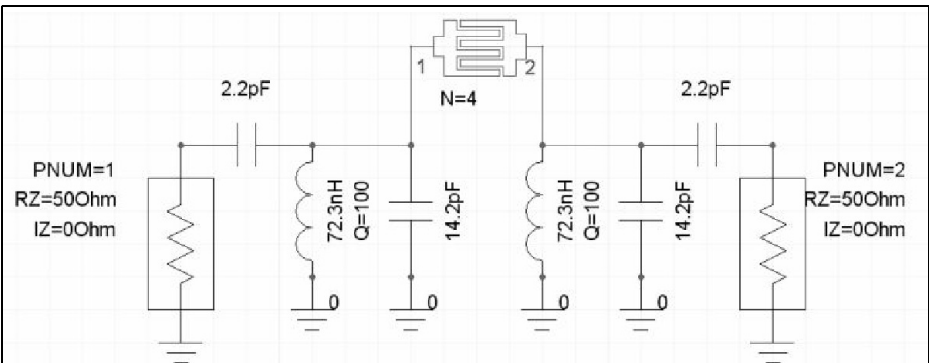


Fig 9: The discrete 0.3pF coupling capacitor is replaced by interdigital capacitor.

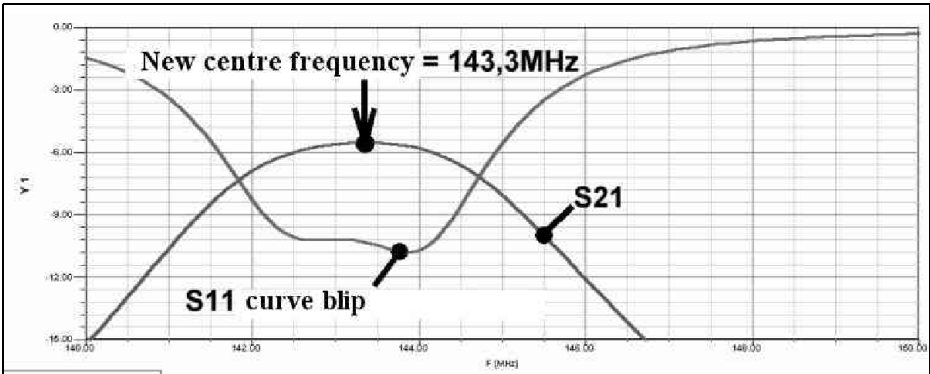


Fig 10: The centre frequency has, as expected, moved lower and there is a diagonally dip in the S11 curve.

response of the capacitors. Probably an alternative circuit diagram with only 3 capacitors can be imagined but the effect is more complex because it can be seen on the finished PCB. The effect can be lived with so the easy solution is just to move the centre frequency to the required value of 145MHz.

The parallel capacitors must be reduced to $13.8\text{pF} = 12\text{pF} + 1.8\text{pF}$, using standard values that can be connected in parallel. The remaining adjustment is to fine tune the two coils using the adjustable cores. The new inductances of $L = 72.3\text{nH}$ corresponds to the simulation result shown in Fig 10.

But this is not the conclusion because the PCB layout and its influence must be considered. Fig 11 shows the PCB layout

that is principally a 50Ω microstrip line. It starts on the left (at the input SMA connectors) with a gap for the 2.2pF SMD coupling capacitor followed by the resonant circuit. The interdigital capacitor is in the centre and the right half is a mirror image of the left hand side. This corresponds to an additional conductor length of approximately 40mm for the circuit and this has the following consequences:

- Four additional sections of 50Ω microstrip line (with a width of 1.83mm for the given PCB data) must be added to the Ansoft Designer SV circuit if the simulation is to agree with the reality.
- The lengths of the pieces of line are $2 \times 13\text{mm} = 26\text{mm}$ (from the SMA connector to the 2.2pF coupling ca-

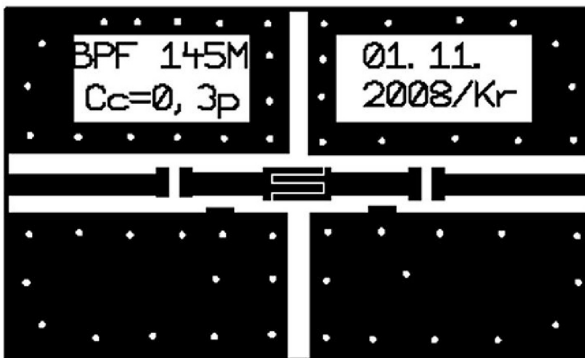


Fig 11: The printed circuit board measures 30mm x 50mm made from Rogers RO4003 with a thickness of 0.813mm.

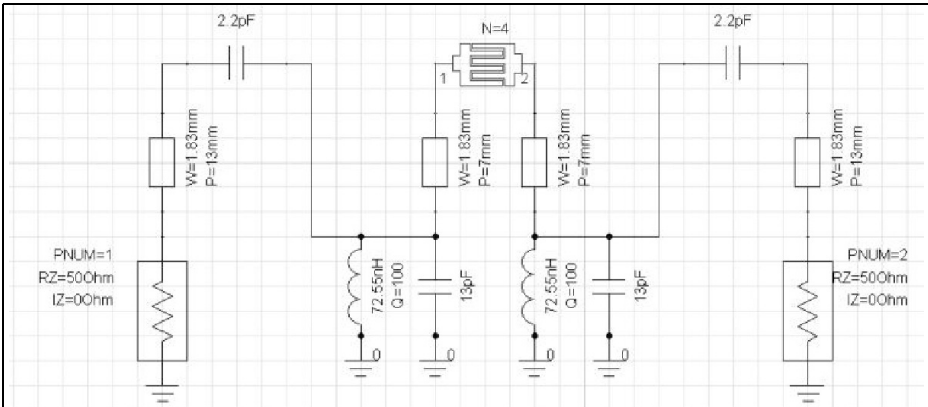


Fig 12: The sections of microstrip line are included into the simulation to reflect the real circuit.

pacitor) and $2 \times 7\text{mm} = 14\text{mm}$ (from the resonant circuit to the interdigital capacitor).

Fig 12 shows the circuit. At these relatively low frequencies the microstrip line detunes capacitors so the parallel components must be adjusted again. Doing this gives the simulation results shown in Fig 13. The simulation of the wider frequency range from 100MHz to 200MHz is shown in Fig 14. Finally it is time to prepare the prototype PCB, the result after some hours of work are shown in Fig 15.

About 50 0.8mm hollow rivets were used for the plated through holes from the ground islands to the continuous lower ground surface. The SMD capacitors and coils are soldered and copper angles are screwed on to fit the SMA sockets. The adjustment cores of the coils are now easily accessible and from experience it is known that nearly no further adjustments are necessary when fitting the PCB into a machined aluminium housing.

The truth comes with the comparison of the curves of Fig 13 and 14 with the image that the network analyser produces from the prototype.

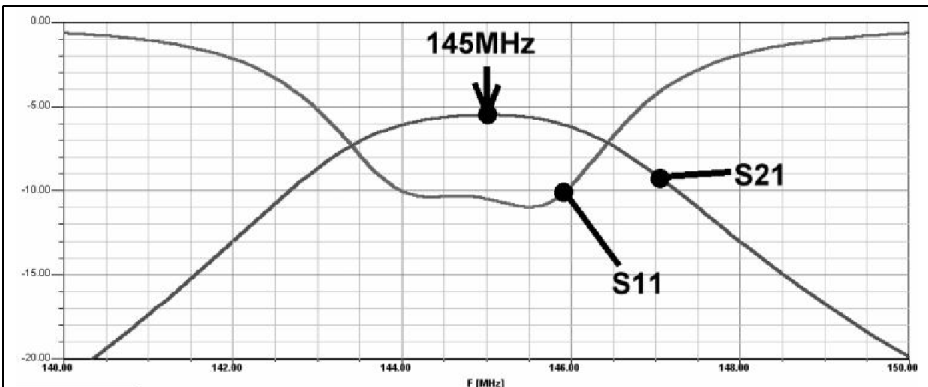


Fig 13: If the results of measurement look the same as this simulation result the final goal will be achieved.

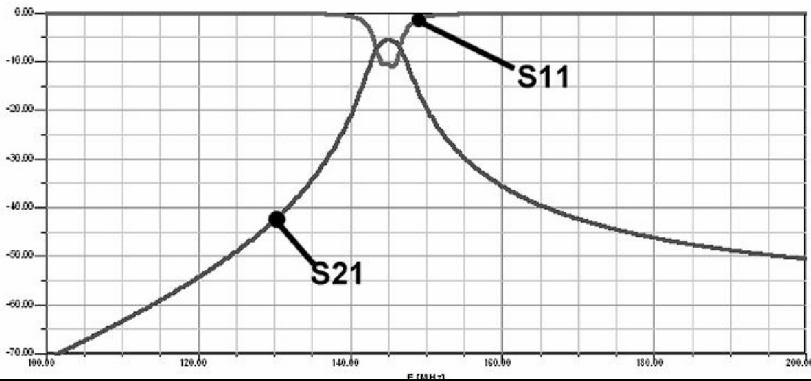


Fig 14: The wider frequency range between 100MHz and 200MHz does not give cause for objection.

By the way: the tear on the PCB that can be seen in Fig 15 was caused by human error. It is hard work fitting so many small rivets and takes some hours. But afterwards when finishing the PCB with a file in a hurry to see the results, too much pressure was applied. So you find out that RO4003 material can be drilled and milled but protests when it meets a stronger opponent. More care needed in future.

3.4. Results of measurement on the prototype

The measurements gave some unpleasant surprises shown in Fig 16, which is the S21 transmission curve (measured after correct alignment) and the simulation from Fig 13. The first mystery is that the

attenuation has risen from 5.5 to 7dB at the centre frequency.

There are some doubts about the method devised to measure the value of the coupling capacitor even though the author is proud of the technique devised. So the best was to look for an owner of the APLAC simulation software (full version). APLAC has a text based command line simulator that can directly compute the value of an interdigital capacitor and the two "end capacitors". Entering the mechanical data for our capacitor design into APLAC and waiting for the result gave great relief because it gave a value of 0.29pF that is very close to the 0.3pF aimed at with Ansoft Designer SV. The interdigital capacitor is probably not the cause of the discrepancy but the sceptical



Fig 15. The simulation converted into a prototype with SMA connectors. The circuit must now be measured on the network analyser.

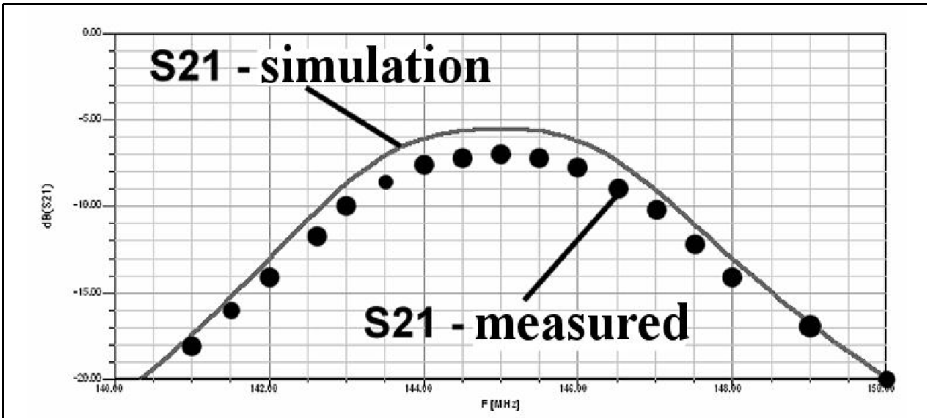


Fig. 16: The measured S21 response shown with the simulation.

developer leaves nothing to chance. The effect of changing the finger length by 0.2mm, and thus the coupling capacity, on the filter curve is shown in Fig 17. This gives the all-clear signal because the frequency range of the transmission curve only changes slightly but the attenuation is not affected.

This leaves the parallel coils as the possible problem (once again) because the NP0 material used in the SMD capacitors is above suspicion at these frequencies. Therefore the coil quality

must be worse than shown on the data sheet ($Q = 130$) and the reason could be because the inductance is adjustable using a brass core. Eddy currents induced in the core oppose the magnetic field to reduce the inductance but unfortunately the quality falls. The quality $Q = 130$ specified, only applies when the core is fully unscrewed and thus almost ineffective, giving the maximum inductance value. There is no mention of this in the data sheet.

This explains everything but to double

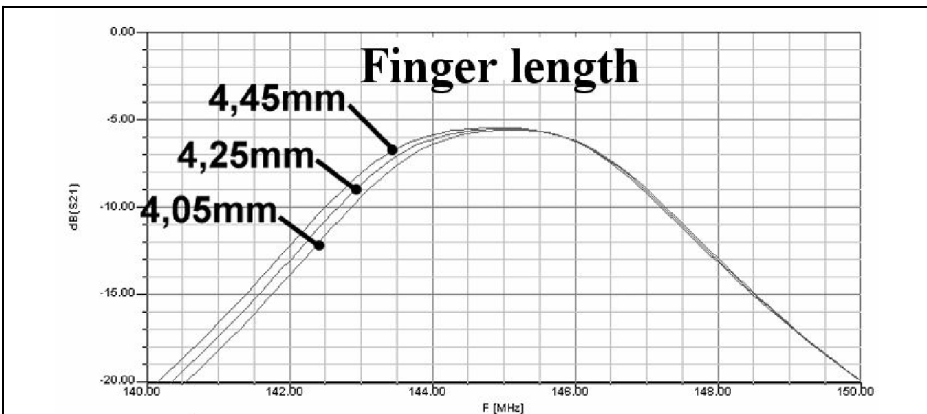


Fig. 17: Different finger lengths and therefore different coupling capacitor values only move the centre frequency of the transmission curve but have no influence on the attenuation.

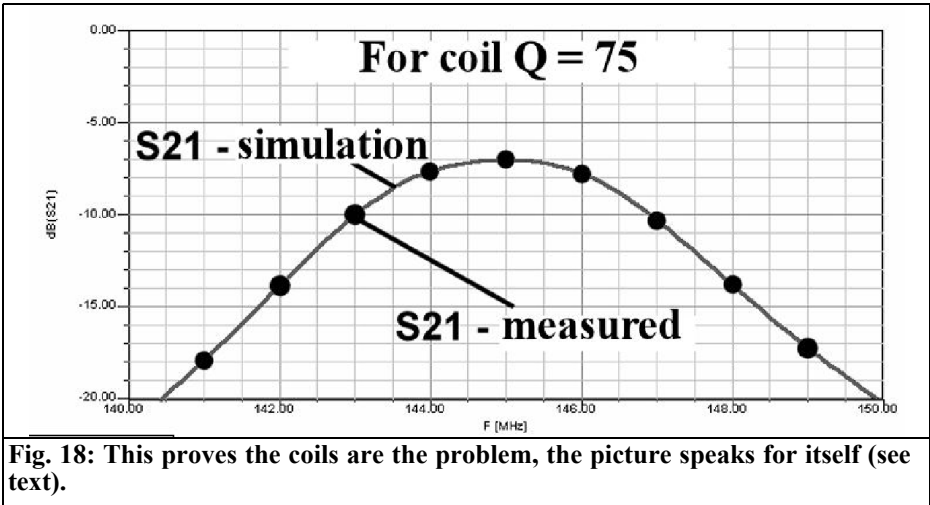


Fig. 18: This proves the coils are the problem, the picture speaks for itself (see text).

check a further simulation was performed. Fig 18 shows the proof because with $Q = 75$ the simulation follows the measured S21 curve accurately. The measurements also agreed with the wide frequency sweep shown in Fig 14.

3.5. Summary

Interdigital capacitors are a fascinating component; as long as the PCB process has an accuracy of 0.01mm they are a good component for problem free mass

production. Only the coils were a problem, more tests would be required to find a better solution.

After the prototype was built and discrepancies noticed the simulations served as an analysis tool to determine the cause of the errors. This was all at no cost and was fun to do. The author wishes that this has inspired you to use Ansoft Designer SV for your own projects, the appendices give more information for filter design.

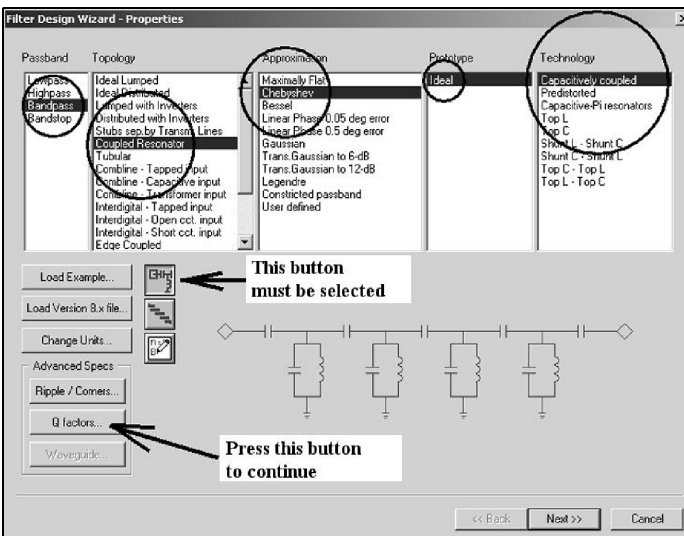


Fig. 19: The start menu for the Filter Tools. Please set all values as shown.



Quality Factors

Properties

- Inductance
- Capacitance
- Transmission line

☐ Ideal, $Q(f) = \text{infinity}$

☐ $Q(f) = Q_o$

☒ $Q(f) = Q_o * f/fo$

☐ $Q(f) = Q_o * \text{sqrt}(f/fo)$

Q_o

fo [GHz]

Test

- IND
- CAP
- SLC
- PLC
- TRL

Freq [MHz]

L [nH]

C [pF]

Zo [ohms]

Length [mm]

Z = 31.415927 + j 6283.185
Y = 0.000000796 - j 0.000159151
|Z| = 6283.264

Fig. 20: The coils need special attention (as always). The quality is set as shown.

4.

Appendix 1: Help for using the filter program in the Ansoft Designer SV

There is no need to continue searching the Internet for suitable CAD software for filter design, because Ansoft Designer SV deals with almost every filter type possible. The problem is how to find the correct selection:

To start the designer with a new file go to the "Project Open" option on the menu and click on "Insert filter Design". Then use something like:

Step 1 (see Fig 19):

In the five menus (from left to right) select: "Bandpass/Coupled Resonator/Chebyshev/Ideal/Capacitively Coupled".

Select the button for "lumped design" (button with circuit diagram). If everything is done click on "Q factors".

Step 2 (see Fig 20):

The coil quality is set to $Q_{min} = 100$ at 100MHz (the filter quality rises linear with frequency). Click OK to return to the previous screen and then click "Next".

Step 3 (see Fig 21):

Now for the serious entry of the filter data:

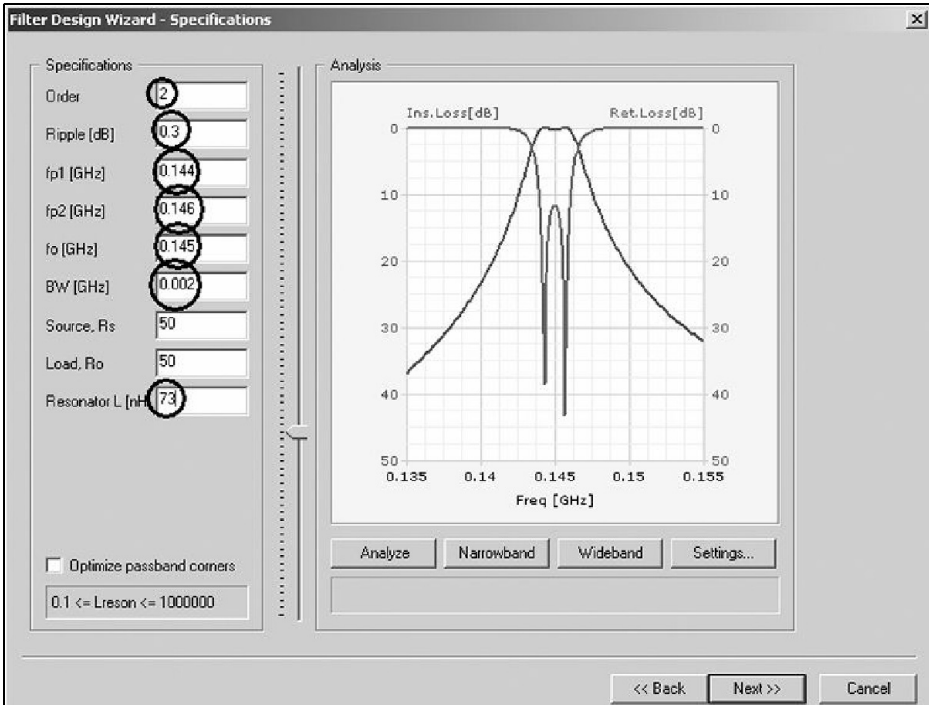


Fig. 21: These are the settings for the filter and should be copied exactly (see text).

Order (filter degree):	2	Source, Rs (source resistance):	50Ω
Ripple:	0.3dB	Load, Ro (load resistance):	50Ω
fp1 (lower cut off frequency):	0.144GHz	Inductor L:	73nH
fp2 (upper cut off frequency):	0.146GHz	(selected parallel inductance,	
fo (centre frequency):	0.145GHz	all the same)	
BW (Bandwidth)	0.002GHz		

Press “Next” and the circuit is produced,

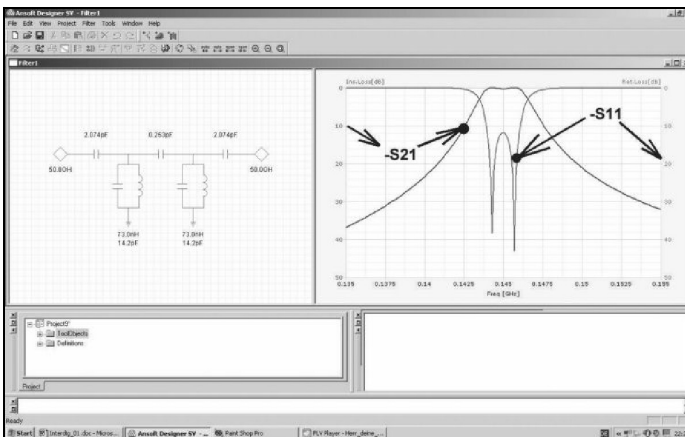


Fig. 22: The circuit and the characteristics of the ideal filter.

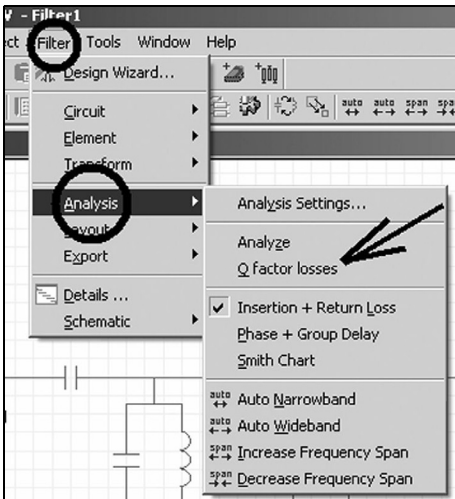


Fig. 23: The addition of the filter quality will distort the characteristics.

then select “Finish”.

Step 4:

Click “Tile vertically” to produce a display of the circuit diagram and associated simulation of S11 and S22 as shown in Fig 22. The vertical axis is marked with “Insertion Loss (dB)” and “Return Loss (dB)”. S11 and S22 are obtained by reversing the sign of these..

Step 5:

To show the effect of the coil quality $Q =$

100 select the view shown in Fig 23 by using the “Filter” menu from the Filter 1 window border and select “Analysis” then “Q Factor Losses”. If a checkmark is set then Fig 24 shows the filter characteristics adjusted for the quality $Q = 100$.

Print the circuit and place it beside the PC because the next appendix needs the component values.

5.

Appendix 2: Simulation of the circuit with the Ansoft Designer SV

Start a new project using the “Insert Circuit Design” option. The “Layout Technology Window” shows: MS-FR4 ($\epsilon_r=4.4$), 0.060 inch, 0.5oz.copper,

At first place the two ports required. Initially they are interconnect ports, double clicking on their circuit symbols gives the chance to change them to Microwave Ports (Fig 25).

Now the remaining components can be found in the Project Window under the “Components/Lumped”. For the capaci-

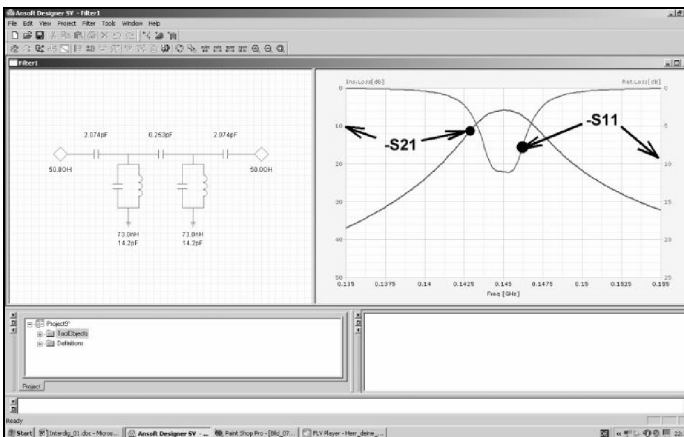


Fig. 24: The filter circuit with a coil quality $Q = 100$.

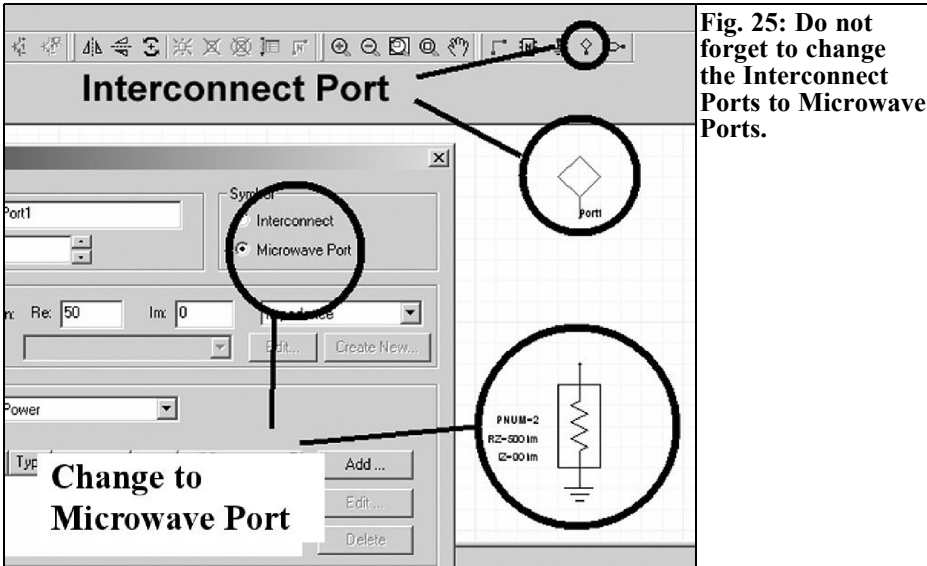


Fig. 25: Do not forget to change the Interconnect Ports to Microwave Ports.

tors a simple “Capacitor” is used but for the coils “INDQ” (Inductor with Q factor) should be used.

and the component values added. Do not forget to double click on the coil symbols and set the quality to $Q = 100$ at 0.1GHz.

The circuit is drawn as shown in Fig 26 using “Wire” to connect the components

The PCB material should be changed to

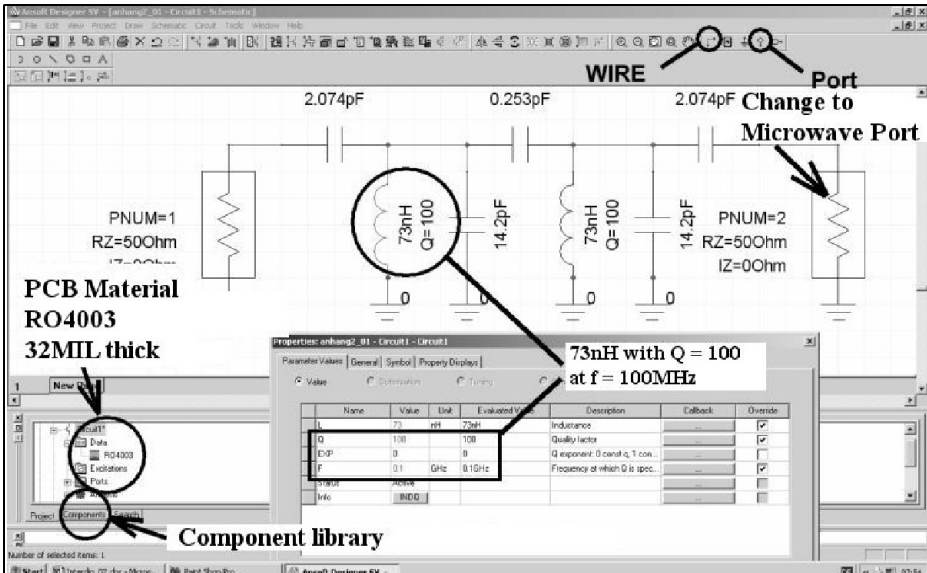


Fig. 26: The simulation circuit shows all the correct components.

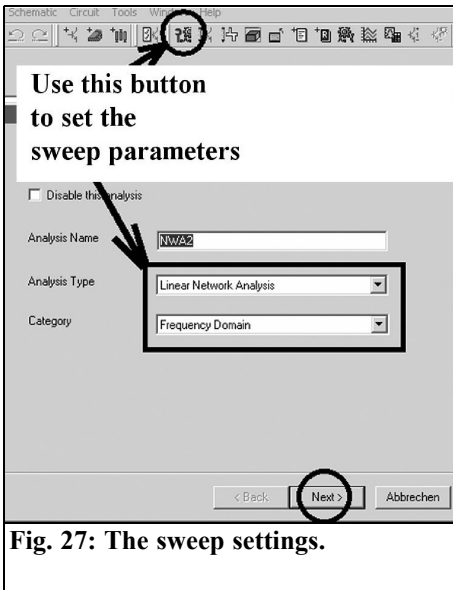


Fig. 27: The sweep settings.

“32MIL = 0.813mm thickness and R04003 material” as described in Fig 6.

Note: When a component is attached to the cursor it can be rotated by pressing “R”. If the component is already placed it can be selected with a single mouse click and rotated by pressing “Control” and “R”.

The circuit is stored under a suitable name and a sweep for 140 - 150MHz in

100kHz steps carried out as shown in Fig 27:

Step 1:

Click the setup button and continue with “Next”.

Step 2:

Select “Add” on the next menu to show the sweep programming (Fig 28) and set the following:

- 1: Control “linear Sweep”
- 2: Sweep attributes (140MHz to 150MHz in 100kHz steps)
- 3: Press “Add”
4. Check the sweep values selected
- 5: Press “OK”
6. Lock the sweep programming with “Finish”

Step 3:

Pressing the simulate button starts the simulation but nothing is displayed until the create report button is pressed (Fig 29). Check that “Rectangular Plot” is selected; this can be changed on the pull down menu, e.g. Smith Chart representation.

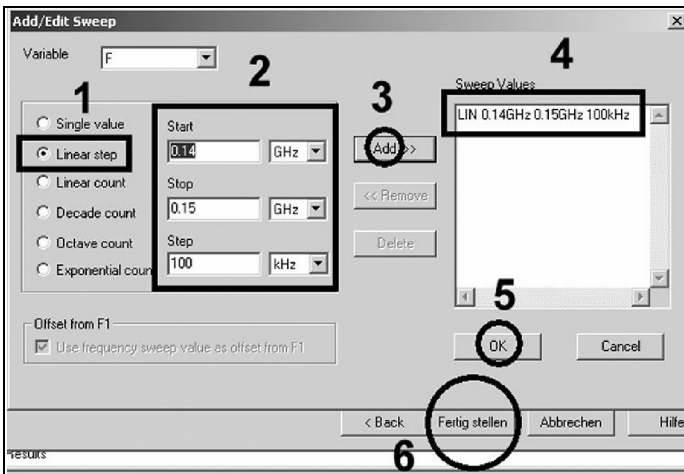


Fig. 28: If everything is correct, the complete sweep can be programmed as this sample.

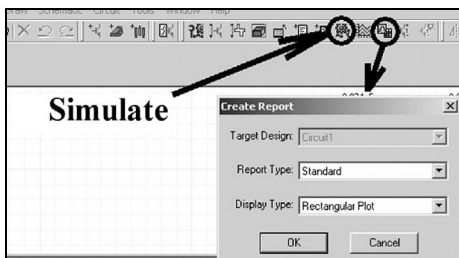


Fig. 29: The display type can also be Smithchart. Also different forms of the representation can be selected.

Step 4:

Use the "Traces" menu to add S-parameters to the list shown in Fig 30. Select S11 and then click "Add Trace". Use the same procedure to add an S21 trace and

press "Done". The display shown in Fig 31 is now produced which is the same as Fig 8. Double clicking on the appropriate axis can change the axis divisions.

6.

Literature

[1] www.elektronikschule.de/~krausg - is the main German web page and:

http://www.elektronikschule.de/~krausg/Ansoft%20Designer%20SV/English%20Tutorial%20Version/index_english.html - is the relevant English page

[2] www.ansoft.com

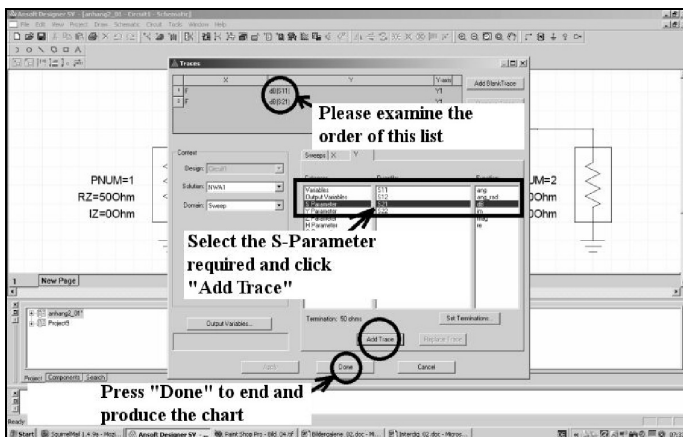


Fig. 30: S11 and S21 are selected for presentation.

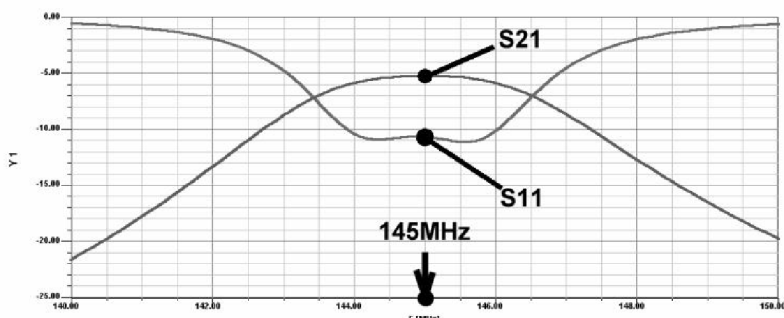


Fig. 31: The simulation result.